ESD-TR-77-281

Technical Note

1977-45

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High-Power, High-Efficiency UHF Amplifier Design

18 November 1977

Prepared for the Department of the Air Force
under Electronic Systems Division Contract F19628-78-C-0002 by

Lincoln Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LEXINGTON, MASSACHUSETTS

The work reported in this document was performed at Lincoln Laboratory, a center for research operated by Massachusetts Institute of Technology, with the support of the Department of the Air Force under Contract F19628-78-C-0002.

This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

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M. L. STEVENS

Group 63

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ABSTRACT

The load-pull technique is shown to be a powerful tool in the design of high-power high efficiency UHF amplifiers. Construction techniques are described which produce high-efficiency amplifiers in the UHF band which require no tuning after assembly. The performance of several amplifiers covering a wide range of output powers is described.

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I. INTRODUCTION

The design of high efficiency UHF and microwave amplifiers has been a cut and try procedure due to the lack of an effective method of determining the optimum load impedance. In the past, high-efficiency amplifiers were achieved by designing tunable narrowband output networks. The amplifier was then tuned for maximum efficiency by a skilled technician or engineer. Because of the complex interactions between gain, output power, and efficiency the tuning procedure itself was a trial and error process. After many hours it was often determined that the optimum efficiency point was outside the tuning range of the output network resulting in a redesign of the matching filter.

This paper describes a design technique based on high-power load-pull measurements[1] which produce very high efficiency fixed tuned amplifiers requiring no retuning after assembly. The load-pull technique described here also gives greater insight into the interaction of gain, output power, and efficiency allowing the design engineer to optimize performance for the parameters important to the application.

Actual load-pull measurements are presented for typical UHF power transistors and the design and construction techniques for a high-efficiency, high-power UHF amplifier are shown. Finally, the measured performance of this and other amplifiers is presented.

II. LOAD-PULL MEASUREMENT

The block diagram in Fig. 1 shows the load-pull measurement set-up. The set-up is essentially the same as used by Pitzalis[2], except that a Tektronix 4051 graphic calculator has been added to allow automatic error correction of power levels and network analyzer data. The tuners which are used on the input and output of the device under test are slotted line tuners constructed of rectangular cross-section, coaxial air lines. The tuning element is a circular disk which may be moved in and out of the line by a micrometer providing a capacitive discontinuity on the line. The disk may also be moved along the length of the line which is approximately $\lambda/2$ at 250 MHz. The tuner

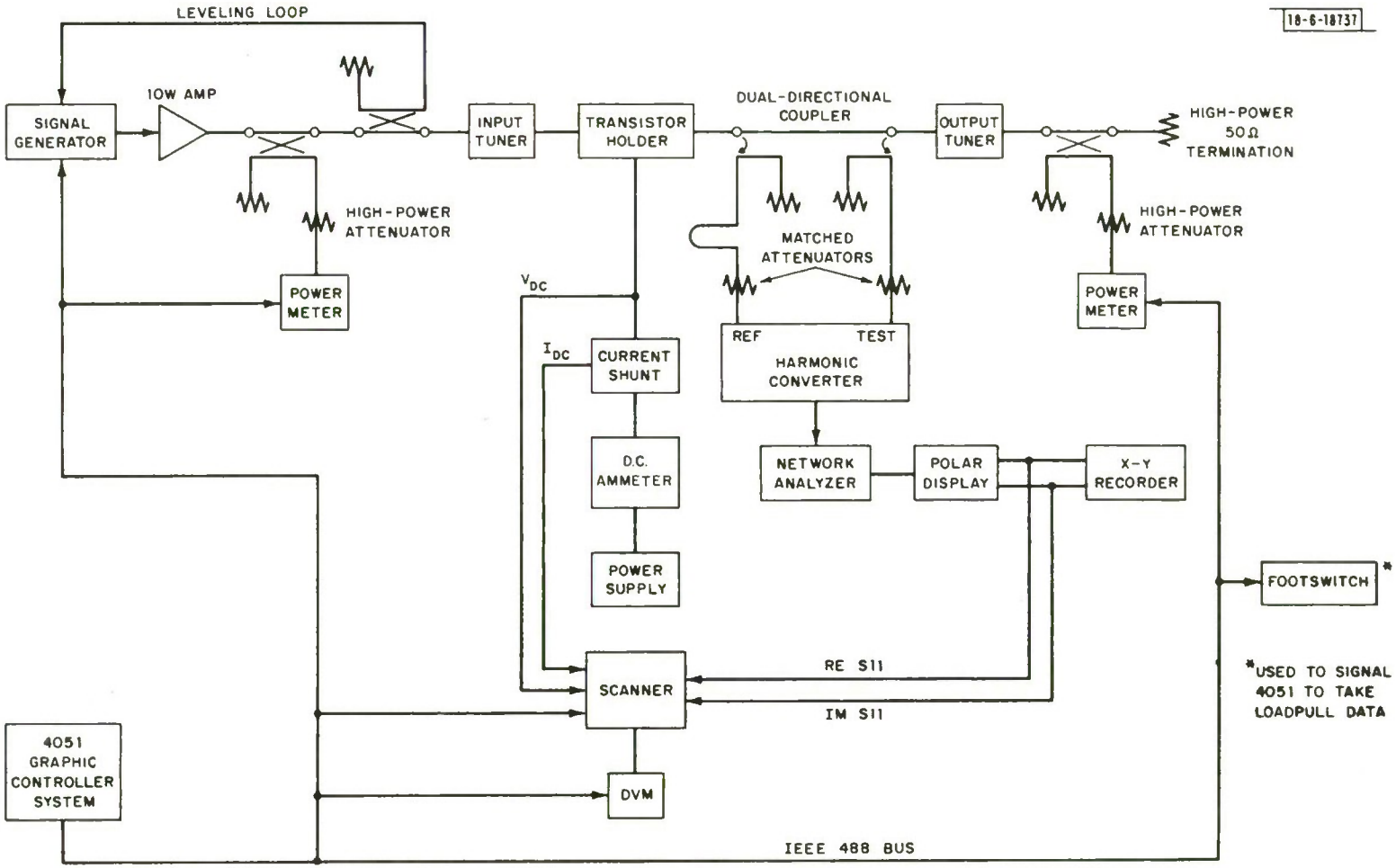


Fig. 1. Block diagram of load-pull measurement set-up.

can provide a VSWR of up to 50:1 at any desired phase angle when operated in the UHF band. The input and output tuners are identical units constructed back-to-back so that all tuning can be performed at one location in the test set-up (see Fig. 2).

The slotted-line topology was chosen for several reasons. First, the capacitive discontinuity in the slotted-line is a low-pass structure which is similar to the low-pass matching filter used in the actual amplifier design. (A low-pass filter structure has been found to be suitable for high-efficiency operation.) Second, the slotted line structure is suitable for automation by using servos or stepping motors.[3] Third, the relationship between the movement of the tuning element and the resulting change in impedance is well defined. The magnitude of the reflection coefficient is changed by moving the capacitive disk in or out. The resulting changes in impedance occur along a constant conductance line of the Smith Chart. Movement of the capacitor along the length of the line causes change in the phase of the reflection coefficient. This makes the slotted-line tuner simple to operate and with a little practice an operator can set practically any desired impedance within a few seconds.

The losses in the tuner remain low out to VSWR's of 10:1. Beyond this value the losses become significiant and inaccuracies occur in the power measurements. Devices requiring load impedances with VSWR's greater than 10:1 are measured in a holder having some low-loss, fixed matching to bring the tuning requirements within the 10:1 VSWR circle on the Smith Chart.

In practice it has been found that devices rated up to 40 watts can easily be measured using the tuner directly. Devices rated at 50 watts or more require a holder with some built in matching circuitry. A typical fixed tuned matching circuit is the single stage low pass filter shown in Fig. 3 which matches 5Ω to 25Ω at 250 MHz.

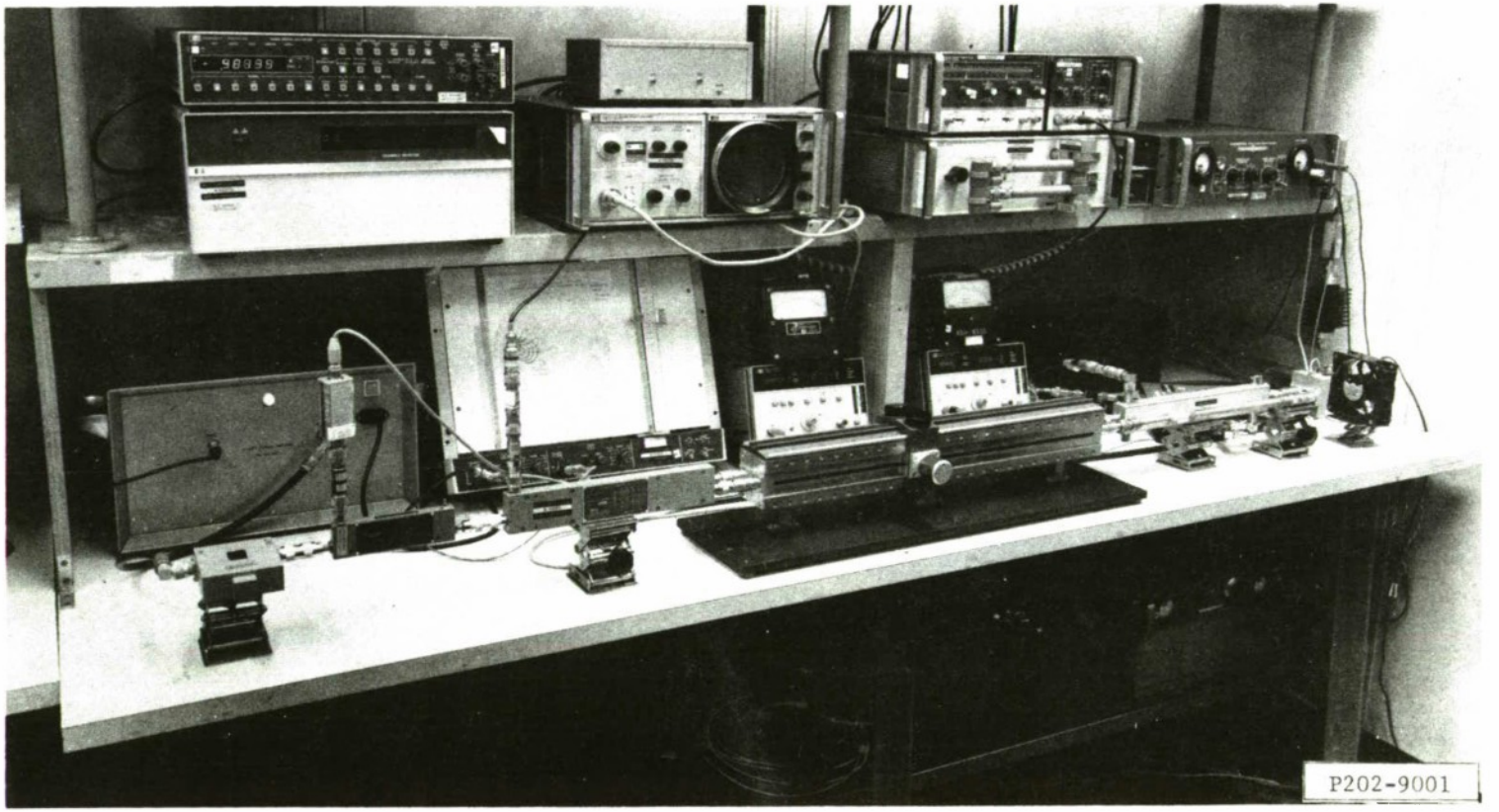
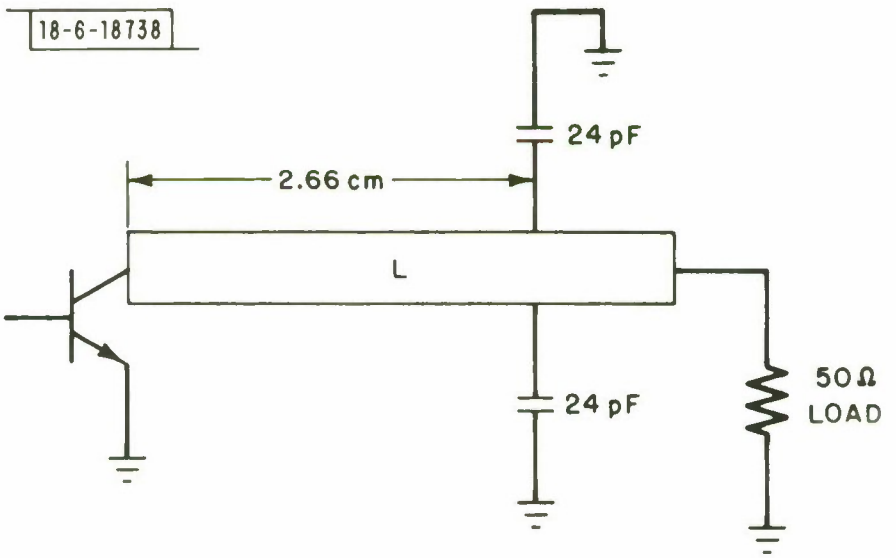


Fig. 2. Load-pull measurement set-up. The double slotted-line tuner is shown at the bottom center of the measurement set-up. The input tuner is on the front side and the output tuner is on the back side. The transistor holder (bottom right) is mounted to an adjustable air line on the input side and the dual-directional coupler on the output side.



L = MICROSTRIP 0.175 in. WIDE ON 1/16 in. TEFLON FIBERGLASS BOARD

Fig. 3. Matched-holder output circuit design. This circuit matches 5Ω to 25Ω at 250 MHz.

III. CALIBRATION

As shown in Fig. 1 the "reference" port of the harmonic frequency converter samples the wave emerging from the output of the device under test. The "test" port of the harmonic frequency converter samples the wave reflected from the slotted line tuner. When properly calibrated, the network analyzer displays the load impedance presented at the collector of the power transistor while the transistor is operating at the desired power level. Any changes in tuning can be seen instantaneously on the network analyzer display and plotted on Smith Chart coordinates using the X-Y recorder, while the resulting changes in RF power output and DC power input can be read on the output power meter and DC ammeter respectively.

A first order calibration of the network analyzer which can be used for setting the visual display and X-Y recorder is made by replacing the transistor to be measured with a copper slug with similar shape and dimensions. The copper slug makes a good reference short in the line at the location of the transistor. The output from the linear amplifier is then fed into the output side of the test set-up, and the line stretcher and CRT display are adjusted to show a short.

There are some errors introduced into the calibration using the method just described which can be partially eliminated if a computer is available to make automatic error correction. The first source of error results because the S_{11} measurement of the short is actually $1/S_{11}$ since the signal source has been moved to the output side of the dual-directional coupler. The second source of error occurs because the dual-directional coupler is not calibrated in the same direction that the measurements are made. These two sources of error and other errors associated with the finite directivity and losses in the coupler are eliminated by incorporating a simple error correction algorithm into a Tektronix 4051 graphic controller which is used to collect the load-pull data. The basic error correction algorithm is contained in a Hewlett-Packard applications note[4]. The algorithm bases the correction on the measurement of a "standard" 50Ω load, a short, and an open. A 50Ω load is measured by replacing the transistor holder with a through line connection,

and the output tuner by a good 50Ω termination. The signal source is fed into the input tuner as shown in Fig. 1. A short and open are measured in the same manner described for the first order calibration except that the dual-directional coupler is reversed by disconnecting it and swapping end for end. The resulting measurements for the short and open are $1/S_{11}$ (short) and $1/S_{11}$ (open) and the reciprocals of these values are used in the correction algorithm. Before load-pull measurements are made the coupler is returned to its original position and the signal source is returned to the input tuner.

IV. LOAD-PULL CURVES

The load-pull curves are produced by applying DC to the transistor under test and a low level CW RF signal at the input tuner. The input tuner is tuned until collector current begins to flow through the device and the output tuner is tuned for maximum power. The power input from the signal source is then increased and the output and input are carefully tuned for maximum gain and power. This process is repeated several times until the output power is one or two dB above the desired operating level. The maximum gain point is then marked on the Smith Chart using the X-Y recorder and the DC current is noted; output power or "gain curves" are then produced by detuning the output until the power drops .2-.5 dB. This point is marked on the Smith Chart. The output is then retuned to a different impedance which produces the same output power and another point is taken. The locus of impedance points producing equal output power is a closed curve on the Smith Chart enclosing the maximum gain point. When the complete circle has been found the output is detuned until the power drops another .2-.5 dB and another curve is generated by repeating the process.

After the curves of constant output power have been determined the output is retuned to the maximum gain point. The output is then detuned again but this time the DC current is held constant. The locus of impedance points producing constant DC current is then determined. Since the supply voltage is also held constant, the constant current curves also represent constant DC input power. Care must be taken to avoid leaving the tuner in the areas where

RF power output is low and DC current is high for more than a few seconds. It is not necessary to take constant current curves at current levels above the value at the maximum gain point, and the constant current curves need not be extended beyond the outer most constant output power curve. Failure to observe these precautions can result in excessive dissipation in the transistor which can weaken the device and cause failure.

Typical load-pull curves for a 30 watt transistor are shown in Fig. 4. The maximum gain point was determined for an output power of 31.9 watts. Constant output power curves were then plotted for 30.8 watts, 28.5 watts, 26.2 watts, and 23.9 watts. Finally, the constant current curves were obtained for 1.84A, 1.7A, 1.5A, 1.3A and 1.1A. The locus of optimum efficiency points can be seen by visual examination of the load-pull curves. The optimum efficiency points lie along a curve originating at the maximum gain point and intersecting perpendicularly both the constant output power curves and the constant current curves.

The maximum efficiency point can be determined by computing the efficiency at several points along the optimum efficiency curve until the peak is found. If the output power is lower than desired at the maximum efficiency point, the input power to the device under test can be increased slightly and a new set of curves can be determined until the desired performance is obtained. The power values indicated on the curves have not been corrected for losses in the tuner or dual-directional coupler because these losses are dependent upon the standing-wave which exists between the tuning capacitor and the transistor and are difficult to determine accurately. The unaccounted losses amount to a few tenths of a dB in most cases. An amplifier which is designed using the load-pull data will usually perform better than the load-pull data predicts because the amplifier output filter will generally have lower loss than the tuner and dual-directional coupler.

Figure 5 shows the load-pull curves for an 80 watt transistor. A transistor holder with the output matching circuit shown in Fig. 2 was used to make the measurement. When a matched holder is used the output connector of the holder is used as the measurement plane. The large set of curves is the

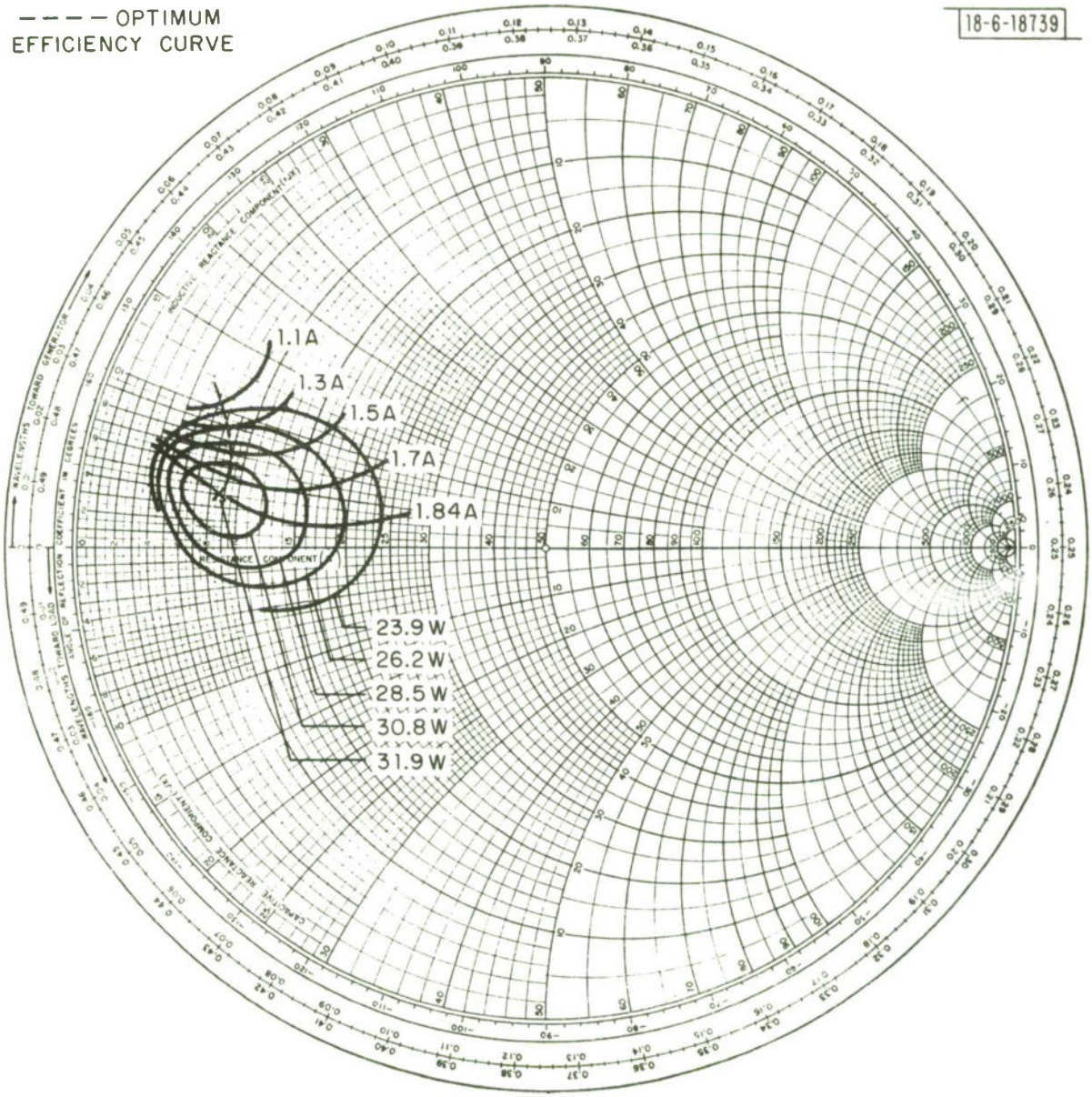


Fig. 4. Load-pull curves for a CD6105 transistor at 250 MHz.

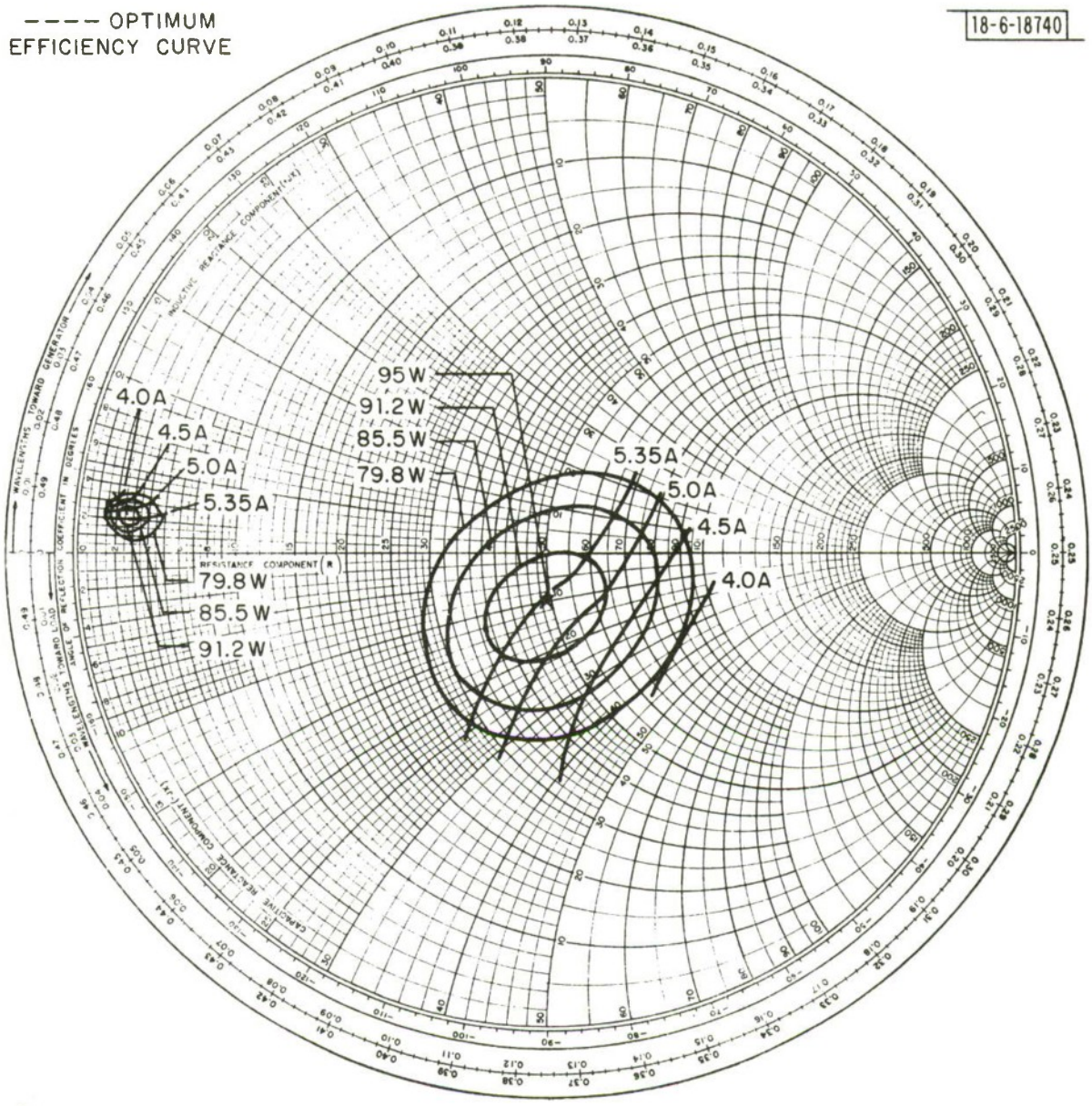


Fig. 5. Load-pull curves for an MRF 327 transistor at 250 MHz. The large set of curves shows the measured values of load impedance at the output connector of the matched holder. The small set of curves shows the load impedance at the transistor.

raw data and shows the impedance values at the output of the holder. The small set of curves is the load-impedance at the transistor. The small set of curves was determined by a computer program which transforms the raw data through the matching filter in the transistor holder.

The transforming equation is:

$$\Gamma_{TRANS} = S_{11F} - \frac{S_{12F}S_{21F}}{S_{22F} + \Gamma_{TUNER}} \qquad (1)$$

where Γ_{TRANS} = reflection coefficient at the transistor

S_{11F}, S_{12F}, S_{21F}, S_{22F} = S-parameters of the matched holder

Γ_{TUNER} = reflection coefficient at the output connector of the matched holder

The computer is also used to determine impedances along the optimum efficiency curve because of the difficulty in reading the Smith Chart values of the transformed curves. The power levels in Fig. 4 also have not been corrected for losses in the tuner, dual-directional coupler or holder. Both Fig. 4 and Fig. 5 were generated without the impedance correction algorithm discussed in the calibration section.

The load-pull curves for the 30 watt CD6105 (Fig. 4) predict the following performance characteristics at 250 MHz

P_{OUT}	COLLECTOR EFFICIENCY	Z_L
31.9 watts	61.9%	8.7 + j4
30.8 watts	68.7%	9.0 + j6.3
28.5 watts	71.2%	9.0 + j8.0
26.2 watts	71.4%	8.5 + j9.0
23.9 watts	71.3%	7.5 + j9.7

Using this transistor, an amplifier was designed to operate at the 26.2 watt level. The construction and performance of this amplifier is discussed in the following section.

The load-pull curves for the 80 watt MRF327 (Fig. 5) predict the following performance characteristics at 250 MHz:

P_{OUT}	COLLECTOR EFFICIENCY	Z_L
95.1 watts	63.5%	2.59 + j2.01
92.9 watts	66.4%	2.54 + j2.34
91.2 watts	67.9%	2.44 + j2.48
87.8 watts	69.7%	2.28 + j2.68
85.5 watts	71.0%	2.14 + j2.81
79.8 watts	70.4%	1.86 + j2.94

Using this transistor, an amplifier was designed to operate at the 85.5 watt level and performance data for this amplifier is also given in the next section.

V. HIGH EFFICIENCY AMPLIFIER DESIGN

Once the maximum efficiency point has been determined on the load-pull curves a simple lowpass output filter is designed which will provide the desired impedance at the transistor when the output is terminated in a 50Ω load. Figure 6 shows the Smith Chart construction used to transform a 50Ω load to an impedance of 8.5 + j9.0Ω at 250 MHz for a 26.2 watt amplifier using the CD6105 transistor.

Several "rules of thumb" have been found useful in producing high performance circuits.

1. 50Ω microstrip transmission lines on 1/16" teflon fiberglass board are used to provide low loss inductances which are rugged and easily reproduced.

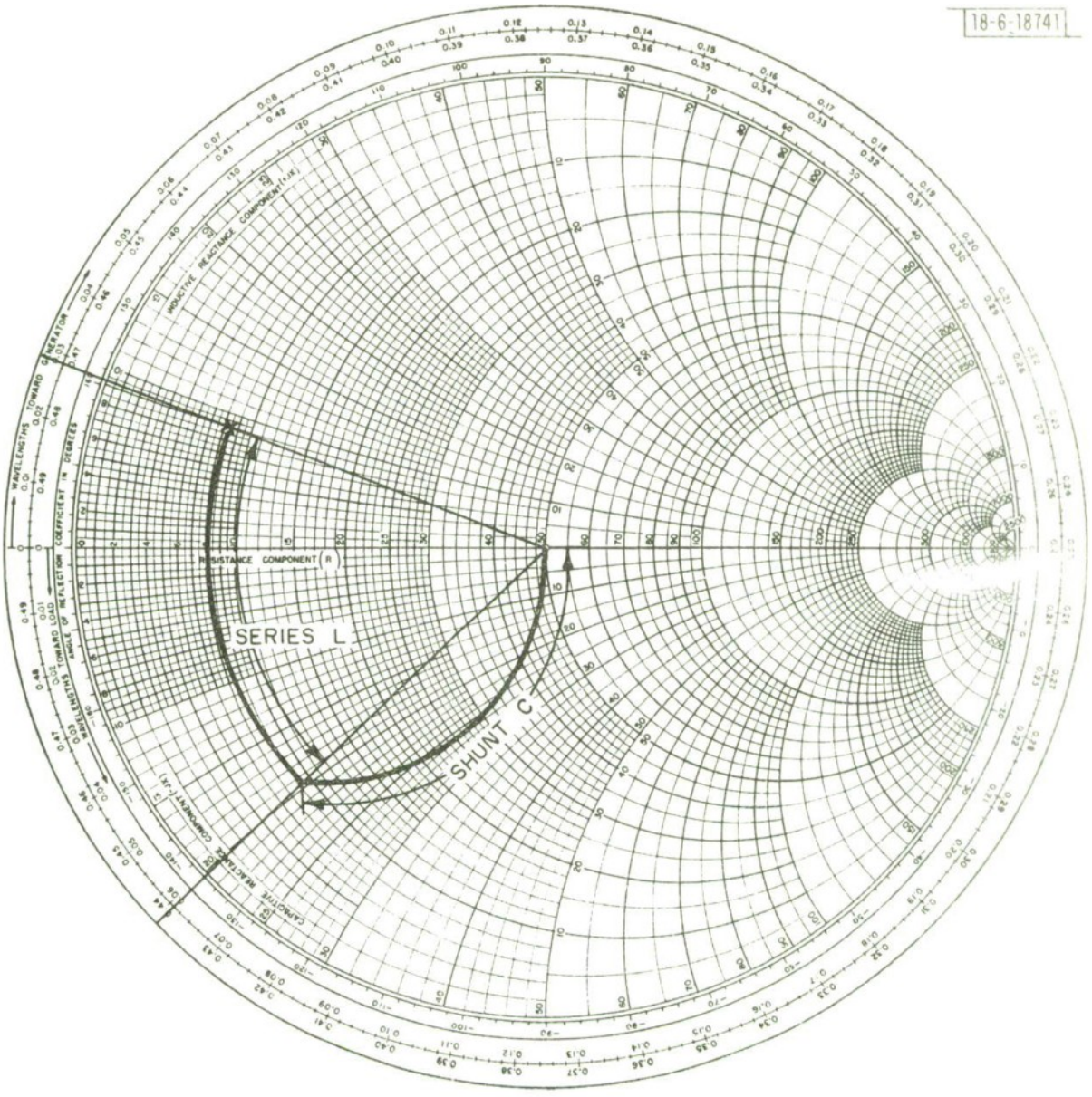


Fig.6. Smith Chart construction for the design of the 26.2 watt amplifier output circuit.

2. Porcelain chip capacitors are used to provide capacitive discontinuities along the line because at UHF frequencies they are the highest Q lumped capacitors presently available. Capacitance values over 50 pF are formed by combining capacitors of smaller value in parallel to reduce the equivalent series resistance that would exist in a single large valued capacitor.[5]

   Distributed capacitors are not used because the capacitance values are relatively large, in most cases requiring prohibitively large areas of printed circuit board.

3. The output matching filters are designed with a Q of 3 or less, even though the amplifier may be used at a single frequency. This is to prevent excessive circulating currents from flowing through the output circuit elements resulting in increased losses and reduced efficiency. The low Q circuits also allow operation of the circuit over a 10% bandwidth with excellent performance as shown in the following section.

4. RF chokes in the collector circuit must have very low DC resistance and high impedance at the operating frequency. A self-resonant coil is used as the RF Choke below 40 watts. Above 40 watts a $\lambda/4$ microstrip transmission line shorted through a capacitor is used as the RF choke.

The inductance required in Fig. 6 for the 26.2 watt amplifier is achieved with a 50Ω microstrip line .0895λ at 250 MHz. A single 27 pF ATC 100 chip capacitor is used to provide the required capacitive discontinuity.

The input circuit is designed to match 1 + j1.5Ω and is only an approximate match to the input of the CD6105. Tables of Chebyshev Impedance Transforming Networks of Low-Pass Filter Form[6] are were used to design the input filter. The approximate input circuit is used to determine the actual input impedance of the device by making a large-signal-S-parameter measurement of the amplifier input impedance. The amplifier input impedance is then transformed back through the input filter to determine the input impedance at the transistor base lead by using Eq. 1. For the purposes of this study, the approximate input filter is used and final tuning on the input is made using the slotted-line tuner.

Figure 7 shows the schematic of the complete amplifier. The breadboard amplifier is constructed as shown in Fig. 8. The printed circuit board is mounted on a large aluminum block which acts as a heat sink. The DC circuitry is in a separate compartment underneath the board.

VI. TEST RESULTS

The amplifier is tested by connecting the output to a high-power 50Ω load. The input is connected through the slotted-line tuner to a 10 watt linear amplifier. A few watts of input power are applied and the input tuner is tuned for maximum gain. No tuning is performed on the output circuit. The gain and efficiency are then measured at several power levels for the frequencies of interest. The test results for the 26.2 watt amplifier using the CD6105 are given below:

FREQUENCY 250 MHz

OUTPUT POWER WATTS	GAIN dB	COLLECTOR EFFICIENCY %
35.8	6.9	75.2
32.4	8.5	83.9
27.8	9.6	86.3
23.9	10.2	83.8
18.6	10.6	77.2

Figure 9 shows the output power, gain, and efficiency plotted as a function of RF input power.

The performance of the 85.5 watt amplifier using the MRF327 is summarized in Figs. 10 and 11.

Figure 10 shows the peak amplifier performance for single frequency operation. In Fig. 10 the RF drive level has been optimized at each frequency to produce maximum efficiency. Figure 11 shows the broadband (10% bandwidth) amplifier performance. In Fig. 11 the RF drive level is constant over the band and has been optimized to produce the flattest gain and power output, with some sacrifice in efficiency.

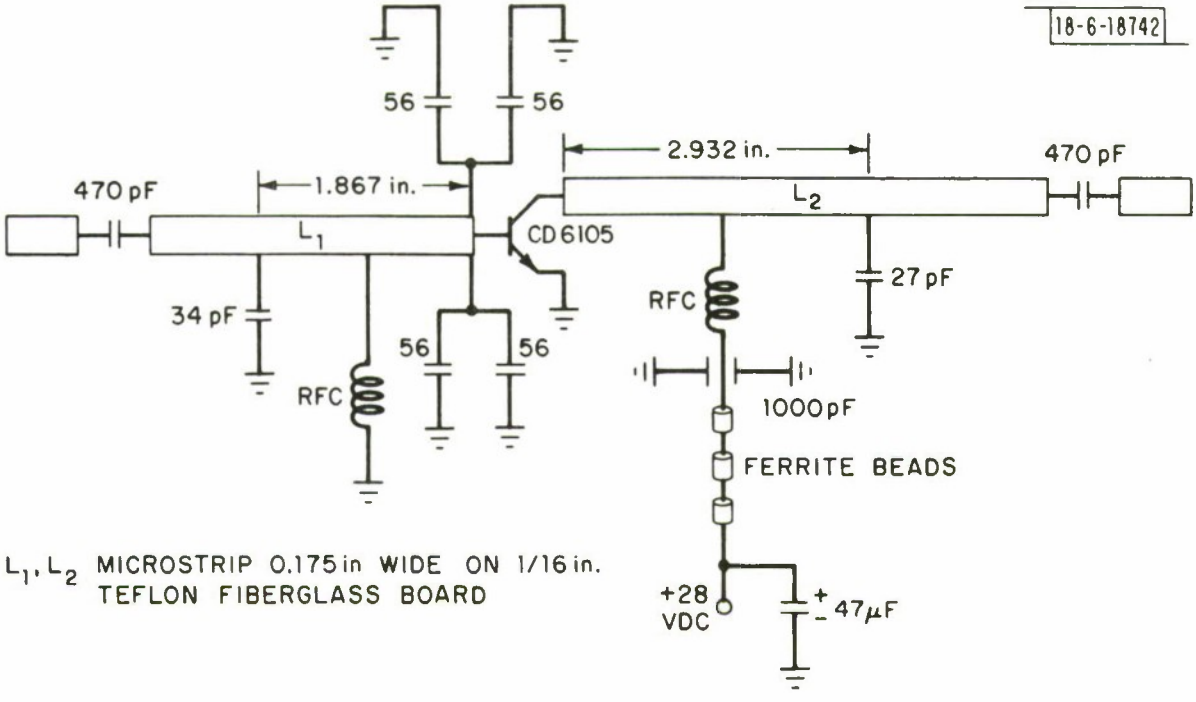


Fig. 7. 26.2 watt amplifier schematic.

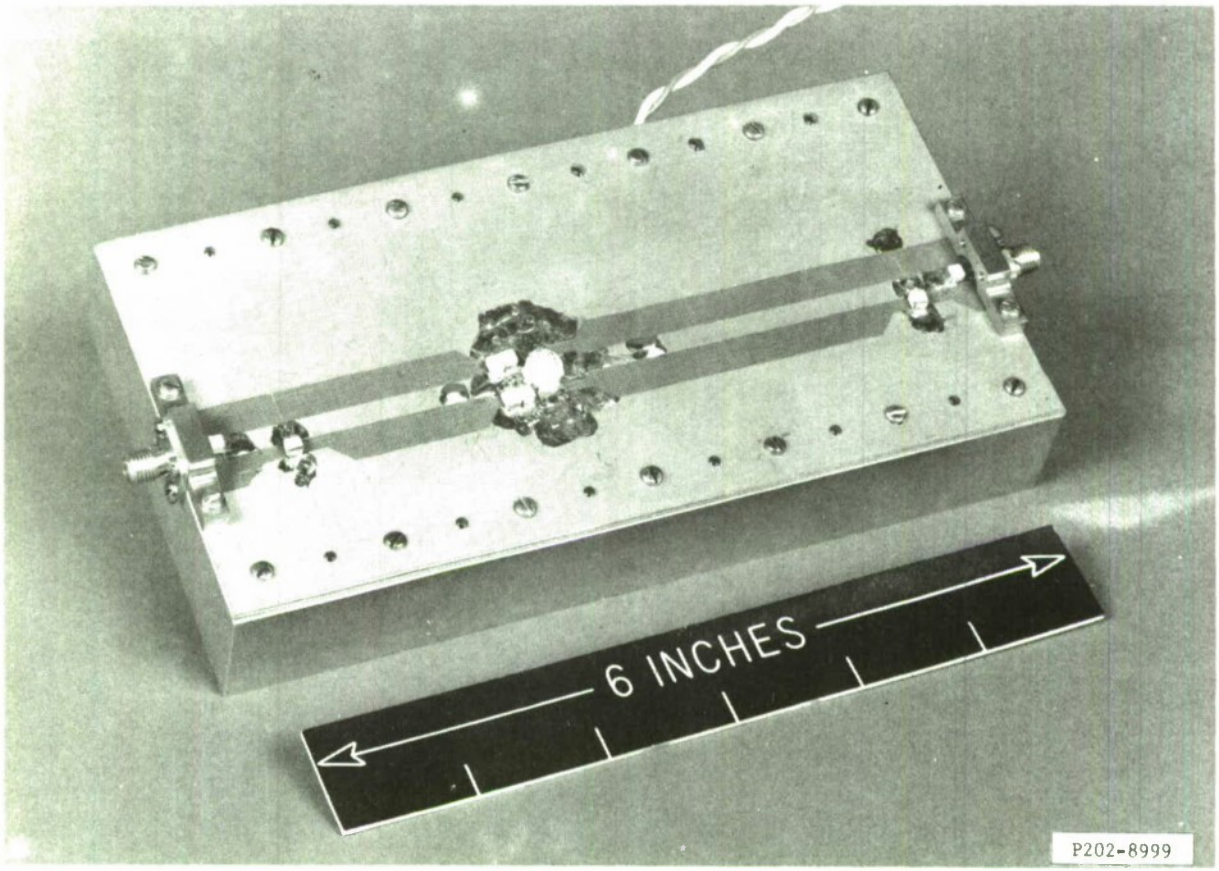


Fig. 8. Breadboard 26.2 watt amplifier. The amplifier input is on the left and the output is on the right. The DC circuitry is in a separate compartment underneath the board.

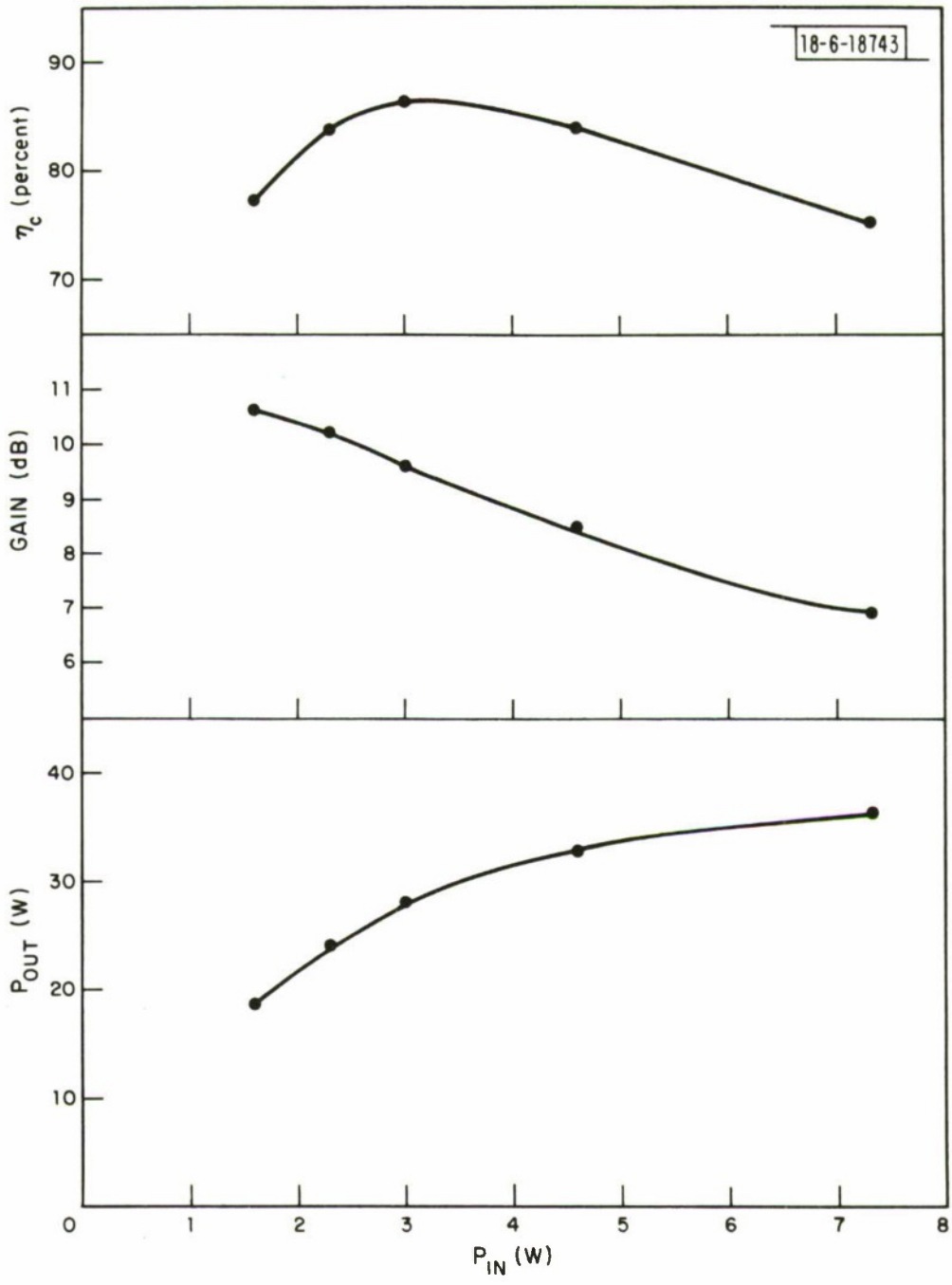


Fig. 9. 26.2 watt amplifier performance versus RF input power. η_c = collector efficiency.

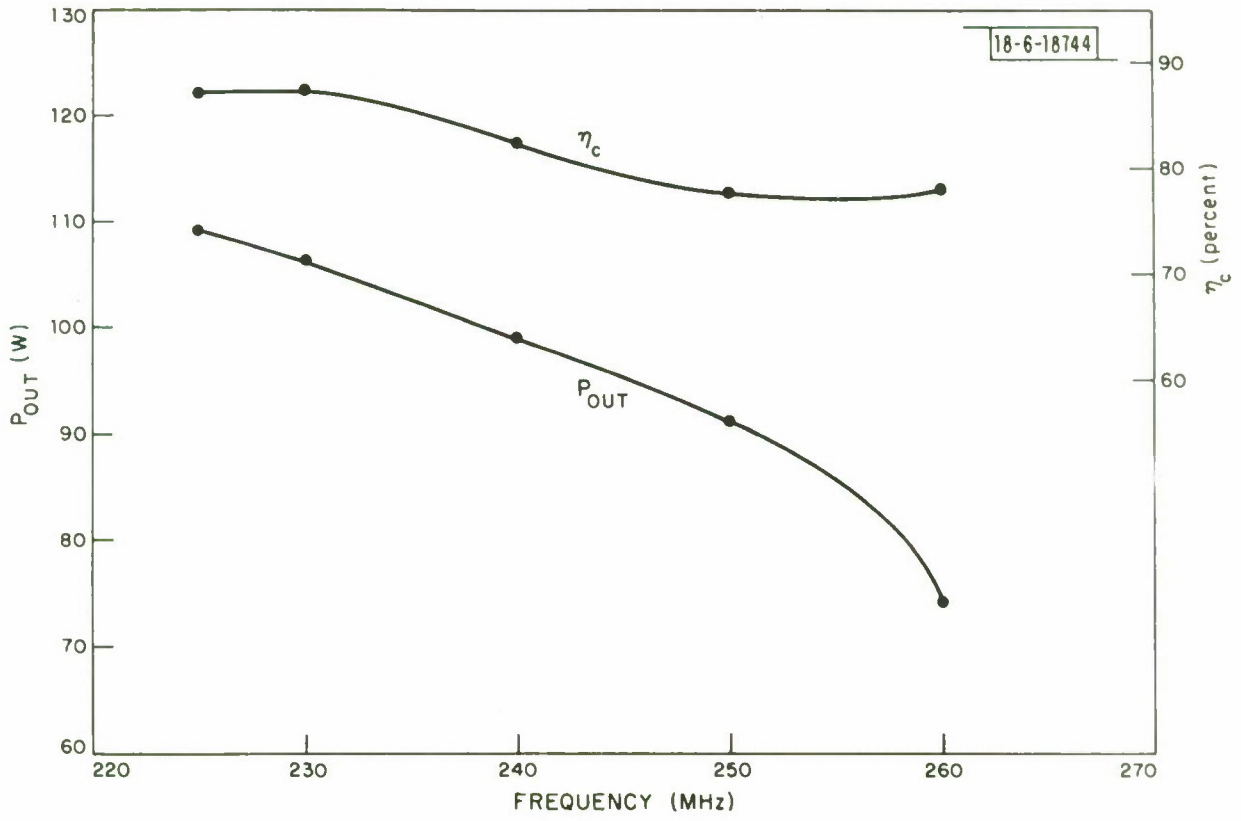


Fig. 10. 85.5 watt amplifier performance for single frequency operation. RF input power has been adjusted to produce maximum efficiency at each frequency.

η_c = collector efficiency.

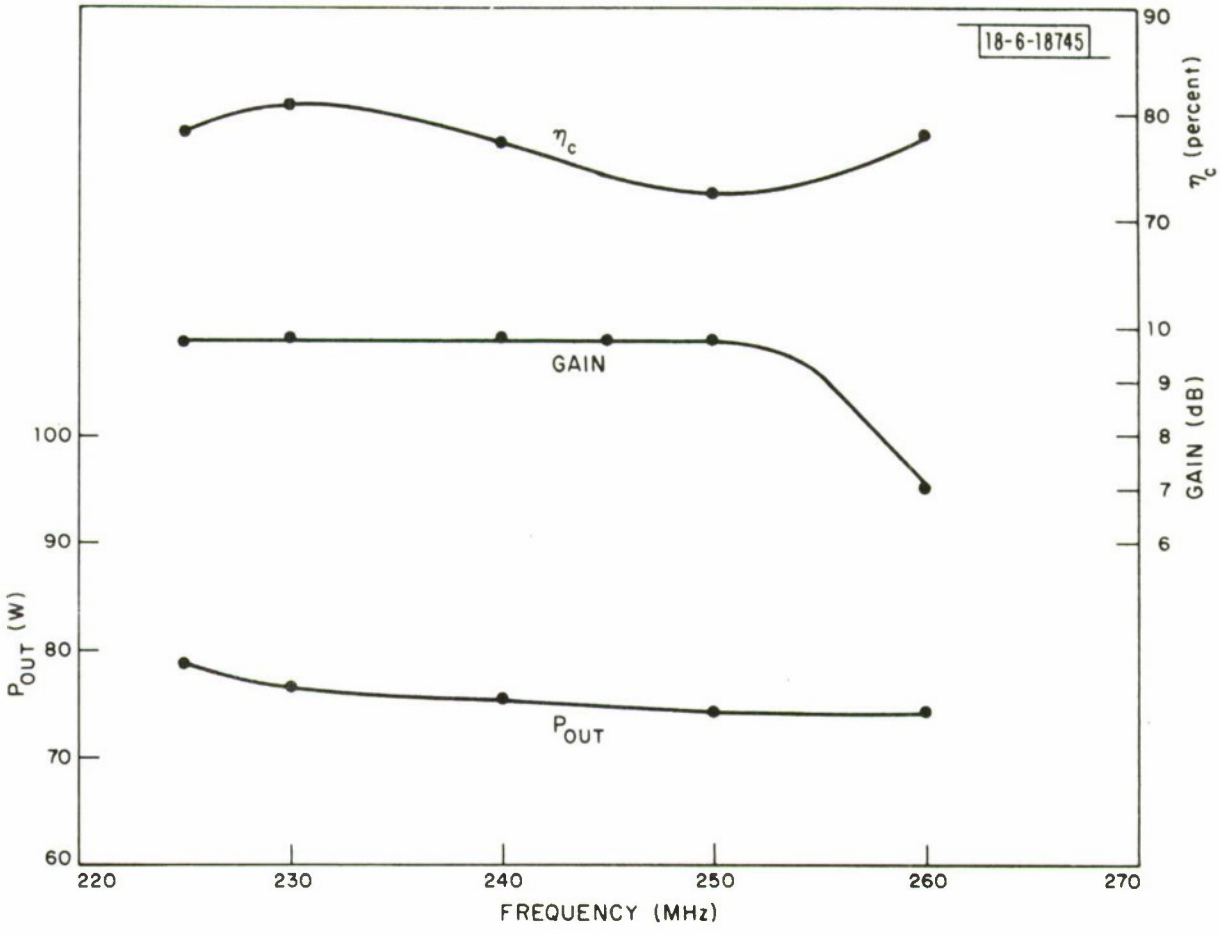


Fig. 11. 85.5 watt amplifier performance for broadband (10% bandwidth) operation. RF input power has been adjusted to produce the flattest gain and RF power output across the band.

η_c = collector efficiency.

TABLE I

PERFORMANCE SUMMARY OF SIX HIGH-EFFICIENCY UHF POWER AMPLIFIERS
DESIGNED USING THE LOAD-PULL TECHNIQUE

DEVICE	FREQ.	PREDICTED		MEASURED		
		POWER OUT	EFFICIENCY	GAIN	POWER OUT	EFFICIENCY
CD6105	250 MHz	26.2W	71.4%	9.6 dB	27.8W	86.3%
C40-28	240 MHz	--	--	8.9 dB	40.9W	86.4%
	250 MHz	32.5W	74.9%	8.1 dB	35.0W	79.7%
	260 MHz	--	--	8.2 dB	30.1W	85.9%
CD1716	240 MHz	--	--	10.5 dB	34.9W	75.1%
(CM45-28)	250 MHz	34.2W	59.6%	9.8 dB	35.8W	79.4%
	260 MHz	--	--	9.7 dB	34.4W	81.4%
2N6439	240 MHz	--	--	7.1 dB	79.7W	88.2%
	250 MHz	62.7W	74.6%	8.1 dB	62.7W	78.3%
MRF327	230 MHz	--	--	7.2 dB	106.2W	87.2%
	240 MHz	--	--	8.6 dB	98.9W	82.3%
	250 MHz	85.5W	71.0%	8.8 dB	91.3W	77.6%
J02016	240 MHz	--	--	8.4 dB	99.1W	81.3%
	250 MHz	108.3W	77.4%	8.2 dB	102.5W	81.7%
	260 MHz	--	--	7.9 dB	80.1W	81.7%

The peak performance of these two amplifiers and four others all using different transistors is summarized in Table 1.

VII. DISCUSSION AND CONCLUSIONS

Table 1 shows a good correlation between predicted and measured output power at the maximum efficiency point for the design frequency of 250 MHz. The efficiency in every case is greater than predicted by the load-pull measurement. As mentioned earlier, this is partly due to the error in the output power recorded during the load-pull measurement because of the unknown losses in the tuner, dual-directional coupler, and transistor holder.

There is, however, in most cases, a peak in the efficiency at or near the design frequency which is higher than can be explained by errors in the load-pull power measurements alone. Snider[7] has pointed out the importance of harmonic terminations for high-efficiency operation at UHF frequencies, and Sokal[8] has discussed output networks which have a specific time response to a step-function input producing very-high efficiencies at lower frequencies. Both techniques stress the importance of output network topology. The load-pull technique described here determines the optimum load impedance at the fundamental frequency only and no attempt has been made to provide specific terminations for harmonics or to provide a specific time response. The simple low-pass filter structure used in the amplifiers described here is seen to be very close to optimum but there may be other topologies that will provide even higher efficiencies. Investigation is continuing along these lines.

One further advantage of the load-pull technique is that transistors can be pre-screened for gain, efficiency and stability. The devices exhibiting the best gain and efficiency can then be selected for critical applications such as satellite transmitters.

Instabilities show up in the load-pull measurements as discontinuities in the curves. Most instabilities are the result of poor test fixture design but devices which are prone to instability can also be detected and weeded out during the screening process.

Load-pull curves are not only useful in the initial design of an amplifier, they can be used to determine how close to optimum the amplifier output filter is. The amplifier can be substituted for the transistor holder and a set of load-pull curves can be made on the complete amplifier. If the amplifier is designed optimally, the optimum efficiency curve will intersect the 50Ω point on the Smith Chart at the maximum efficiency point.

One last observation is that the load-pull curves point out that the optimum termination for high-efficiency always lies on the inductive side of the maximum gain point as shown by Figs. 4 and 5. Furthermore, if the maximum gain point is mapped at the center of an admittance Smith Chart it can be seen that the optimum efficiency curve roughly follows the line of constant conductance into the inductive region of the Smith Chart.

The load-pull technique has been shown to be a powerful tool in the design of high-power high efficiency UHF amplifiers. Construction techniques have been described which produce high-efficiency amplifiers in the UHF band which require no tuning after assembly and the performance of several amplifiers covering a wide range of output powers has been described.

ACKNOWLEDGEMENT

The author wishes to express thanks to Mr. Richard E. Dolbec for the design and construction of the slotted line tuner.

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1. REPORT NUMBER ESD-TR-77-281	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE *(and Subtitle)* High-Power, High-Efficiency UHF Amplifier Design		5. TYPE OF REPORT & PERIOD COVERED Technical Note 6. PERFORMING ORG. REPORT NUMBER Technical Note 1977-45
7. AUTHOR(s) Mark L. Stevens		8. CONTRACT OR GRANT NUMBER(s) F19628-78-C-0002
9. PERFORMING ORGANIZATION NAME AND ADDRESS Lincoln Laboratory, M.I.T. P.O. Box 73 Lexington, MA 02173		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Program Element No. 63431F Project No. 1227
11. CONTROLLING OFFICE NAME AND ADDRESS Air Force Systems Command, USAF Andrews AFB Washington, DC 20331		12. REPORT DATE 18 November 1977 13. NUMBER OF PAGES 32
14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)* Electronic Systems Division Hanscom AFB Bedford, MA 01731		15. SECURITY CLASS. *(of this report)* Unclassified 15a. DECLASSIFICATION DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

18. SUPPLEMENTARY NOTES

None

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

load-pull technique

UHF amplifiers

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The load-pull technique is shown to be a powerful tool in the design of high-power, high-efficiency UHF amplifiers. Construction techniques are described which produce high-efficiency amplifiers in the UHF band which require no tuning after assembly. The performance of several amplifiers covering a wide range of output powers is described.

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SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*